Amendments to the Abstract:

The following Abstract will replace all prior versions of the Abstract in the application:

~~A semiconductor device comprises a memory cell array, a counting circuit, a control circuit, a specification circuit, a selection circuit and a data I/O circuit. The selection circuit effects switching between a normal mode and a synchronous mode in a mode setting cycle. In the normal mode, setting of addresses is performed irrespective of a clock signal. In the synchronous mode, an edge of the clock signal determines the timing of operation.~~ A semiconductor device comprises a memory cell array, a control section and a latency setting circuit. The control section configured to receive a clock signal and a control signal, and configured to output a plurality of data in synchronism with the clock signal after the control signal is asserted. The latency setting circuit configured to set the latency N, and the latency setting circuit including at least one switch which fixes the latency by use of an externally supplied signal.

Remarks

Claims 1-10 were pending in the application. Claims 1-10 have been canceled and new claims 11-36 have been added. No new matter has been added. Therefore, claims 11-36 are pending in the application.

Applicants believe that the present application is in condition for allowance. Examination on the merits is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date 9/26/03

By _____

Glenn Law
Attorney for Applicant
Registration No. 34,371

FOLEY & LARDNER
Customer Number: 22428

22428
PATENT TRADEMARK OFFICE
Telephone: (202) 672-5426
Facsimile: (202) 672-5399